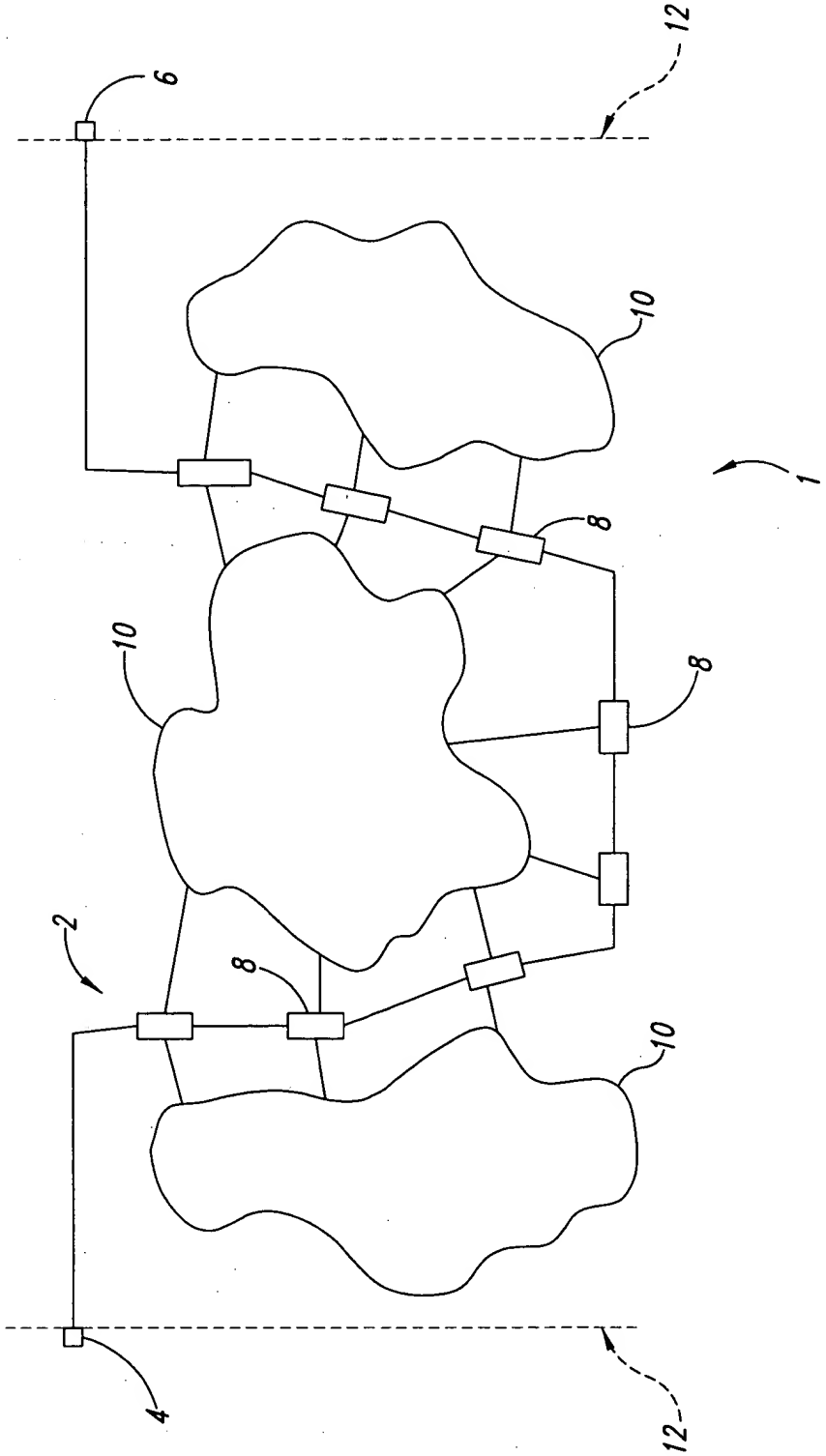


*Fig. 1*
*(Prior Art)*

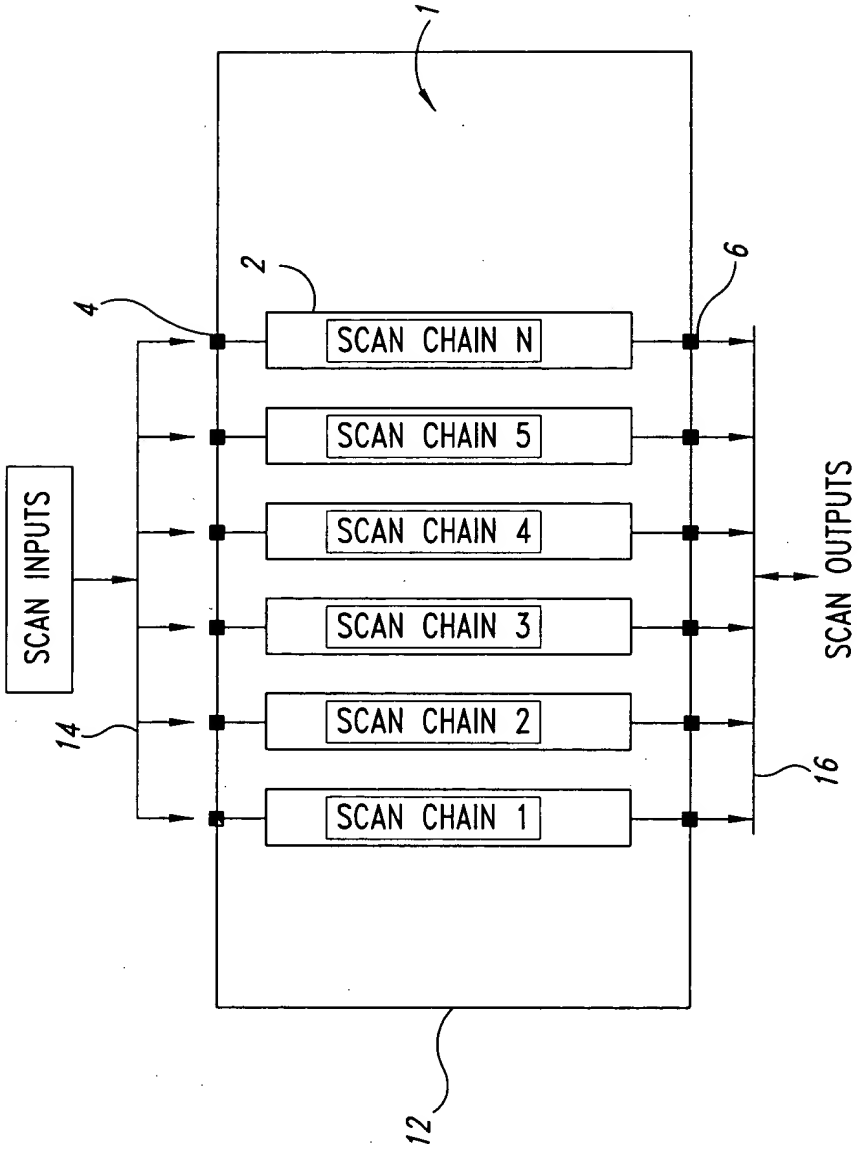


*Fig. 2*
*(Prior Art)*

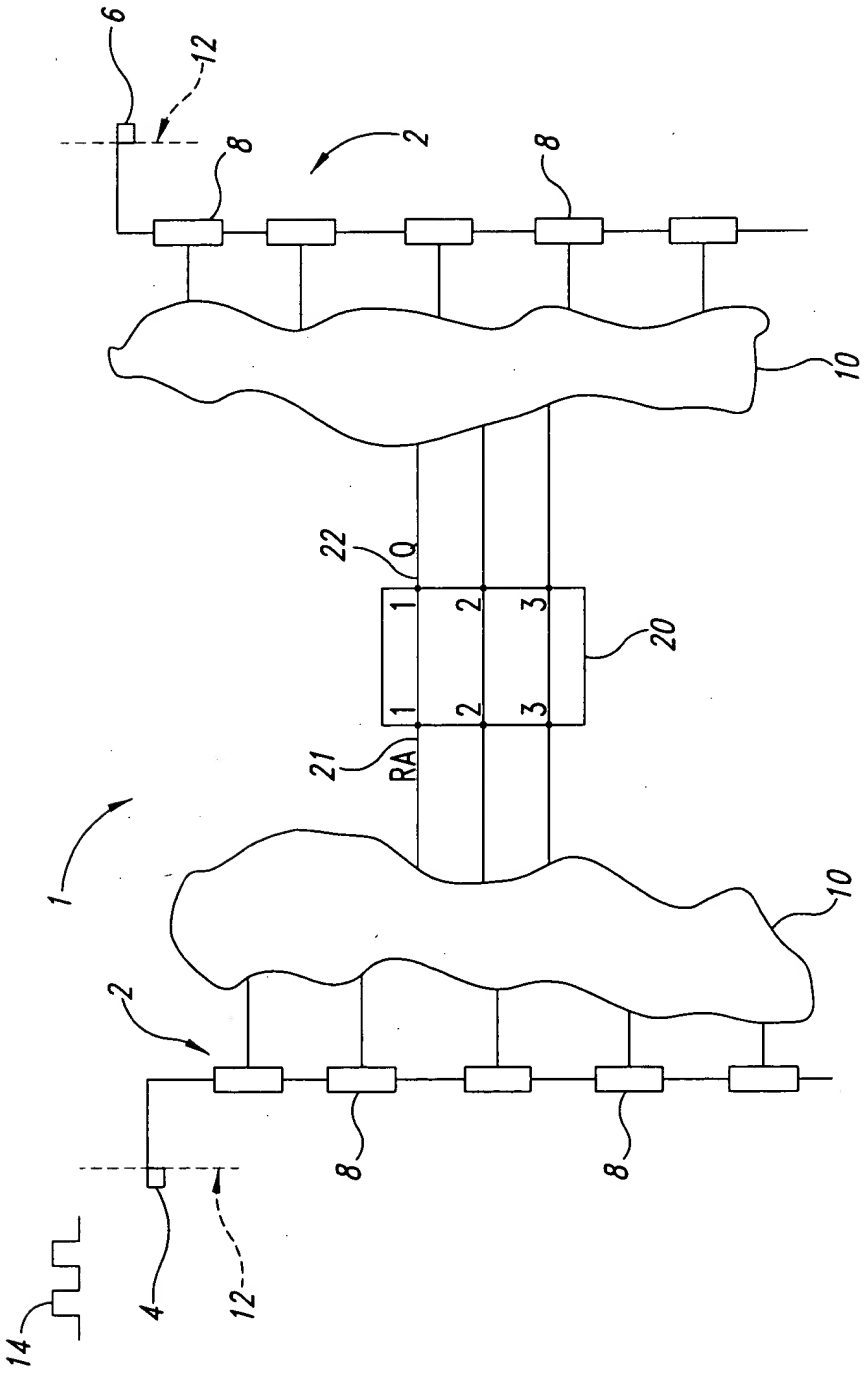


*Fig. 3*
*(Prior Art)*

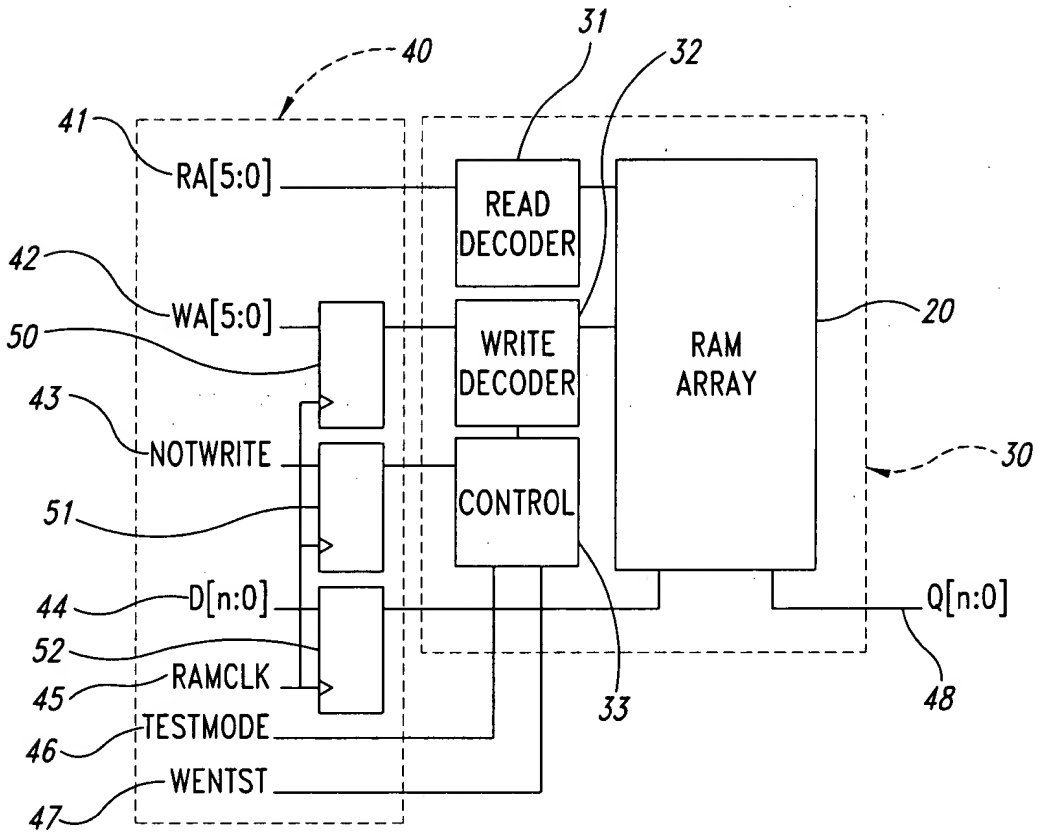
40
31
32
41
RA[5:0]
READ DECODER
42
WA[5:0]
50
WRITE DECODER
RAM ARRAY
20
43
NOTWRITE
CONTROL
30
51
44
D[n:0]
Q[n:0]
52
45
RAMCLK
33
48
TESTMODE
46
WENTST
47

*Fig. 4*

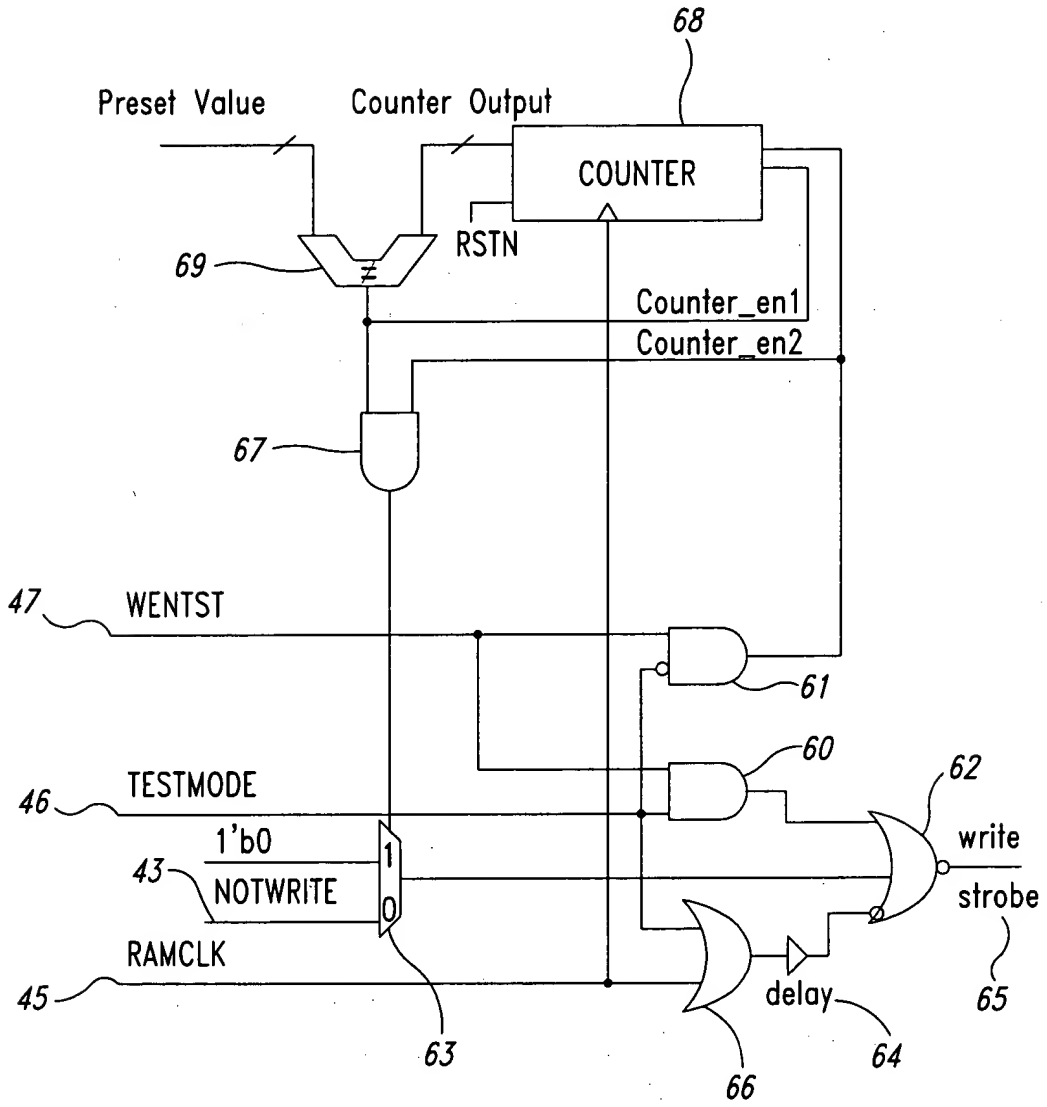
68
Preset Value
Counter Output
COUNTER
RSTN
69
Counter_en1
Counter_en2
67
47
WENTST
61
60
62
46
TESTMODE
1'b0
43
NOTWRITE
1
0
write
strobe
RAMCLK
45
delay
65
63
66
64

*Fig. 5*

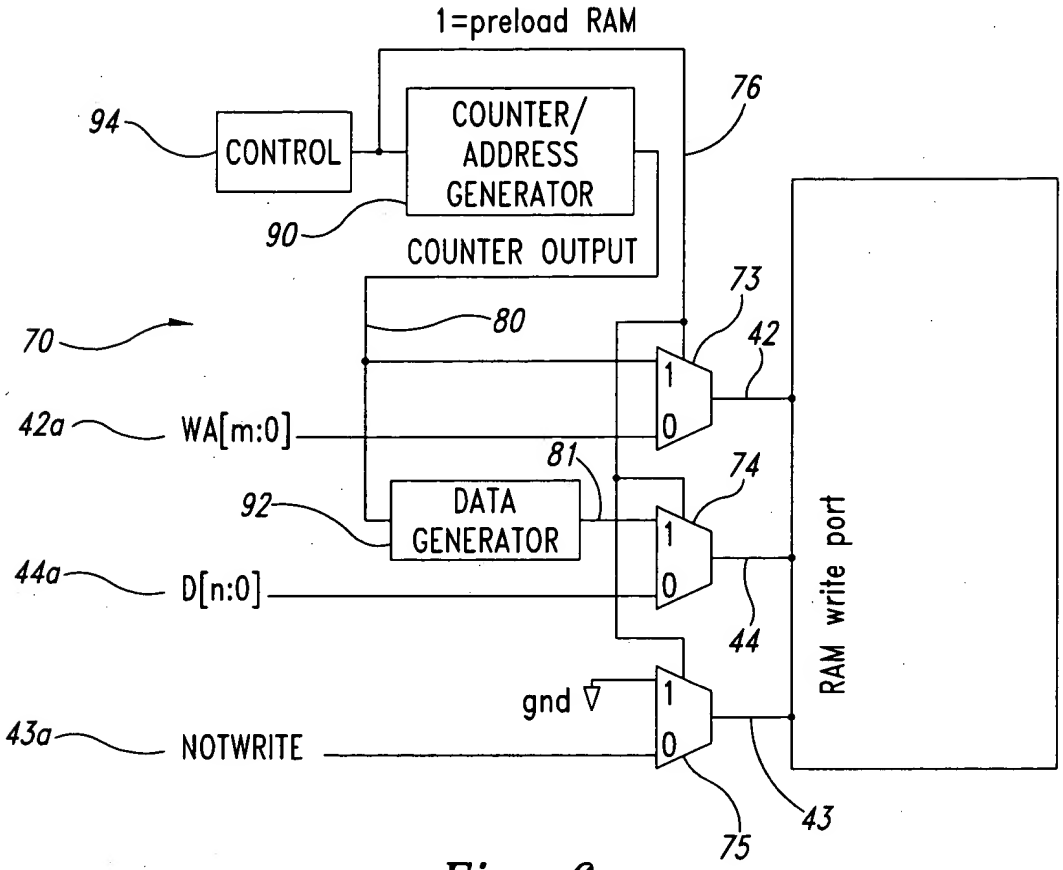


*Fig. 6*

| | data bit 7 | data bit 6 | data bit 5 | data bit 4 | data bit 3 | data bit 2 | data bit 1 | data bit 0 |
|---|---|---|---|---|---|---|---|---|
| address=000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| address=001 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| address=010 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| address=011 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| address=100 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| address=101 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| address=110 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| address=111 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

*Fig. 7*

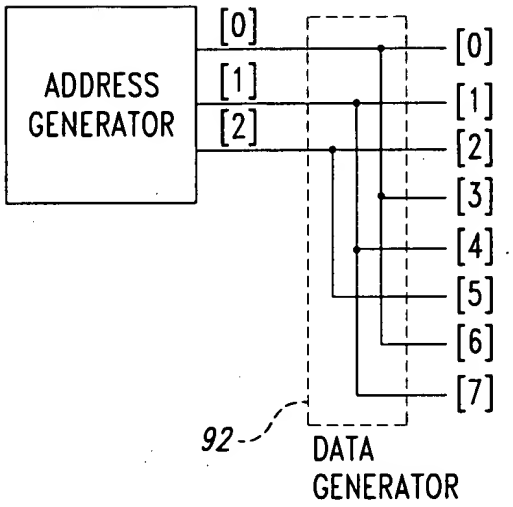
ADDRESS GENERATOR
[0]
[1]
[2]
[0]
[1]
[2]
[3]
[4]
[5]
[6]
[7]
92
DATA GENERATOR

*Fig. 8*

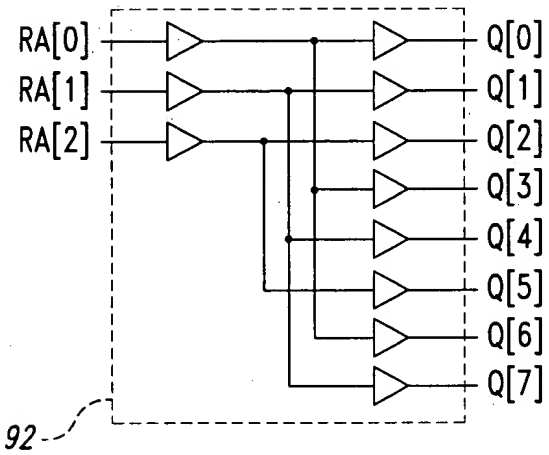
RA[0]
RA[1]
RA[2]
Q[0]
Q[1]
Q[2]
Q[3]
Q[4]
Q[5]
Q[6]
Q[7]
92

*Fig. 9*

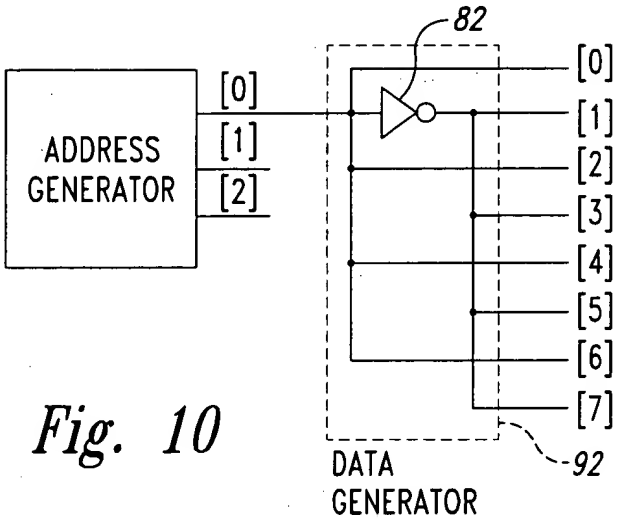
82
ADDRESS GENERATOR
[0]
[1]
[2]
[0]
[1]
[2]
[3]
[4]
[5]
[6]
[7]
92
DATA GENERATOR

*Fig. 10*

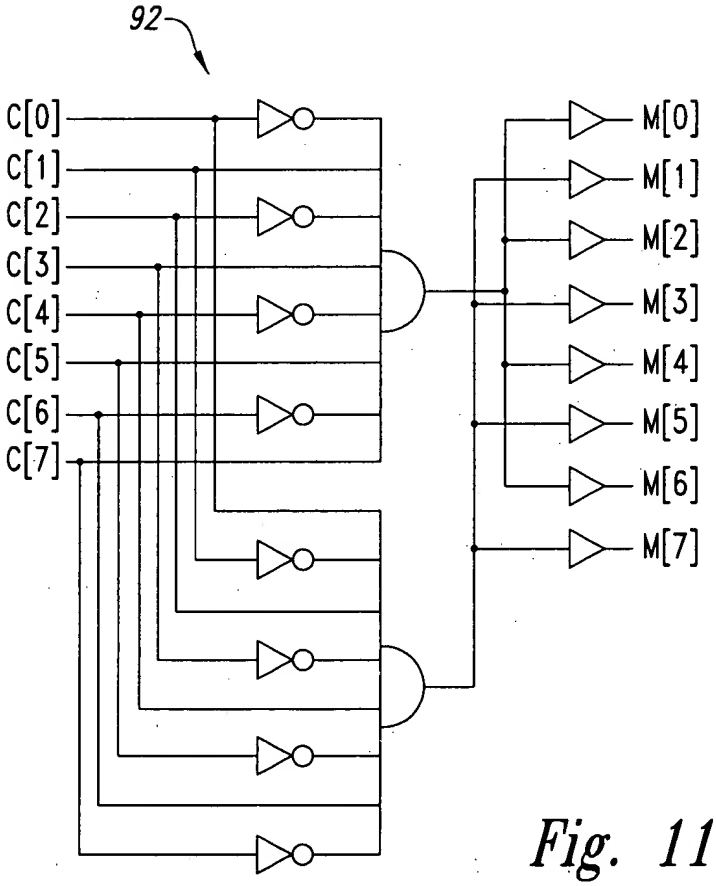
92
C[0]
C[1]
C[2]
C[3]
C[4]
C[5]
C[6]
C[7]
M[0]
M[1]
M[2]
M[3]
M[4]
M[5]
M[6]
M[7]

*Fig. 11*

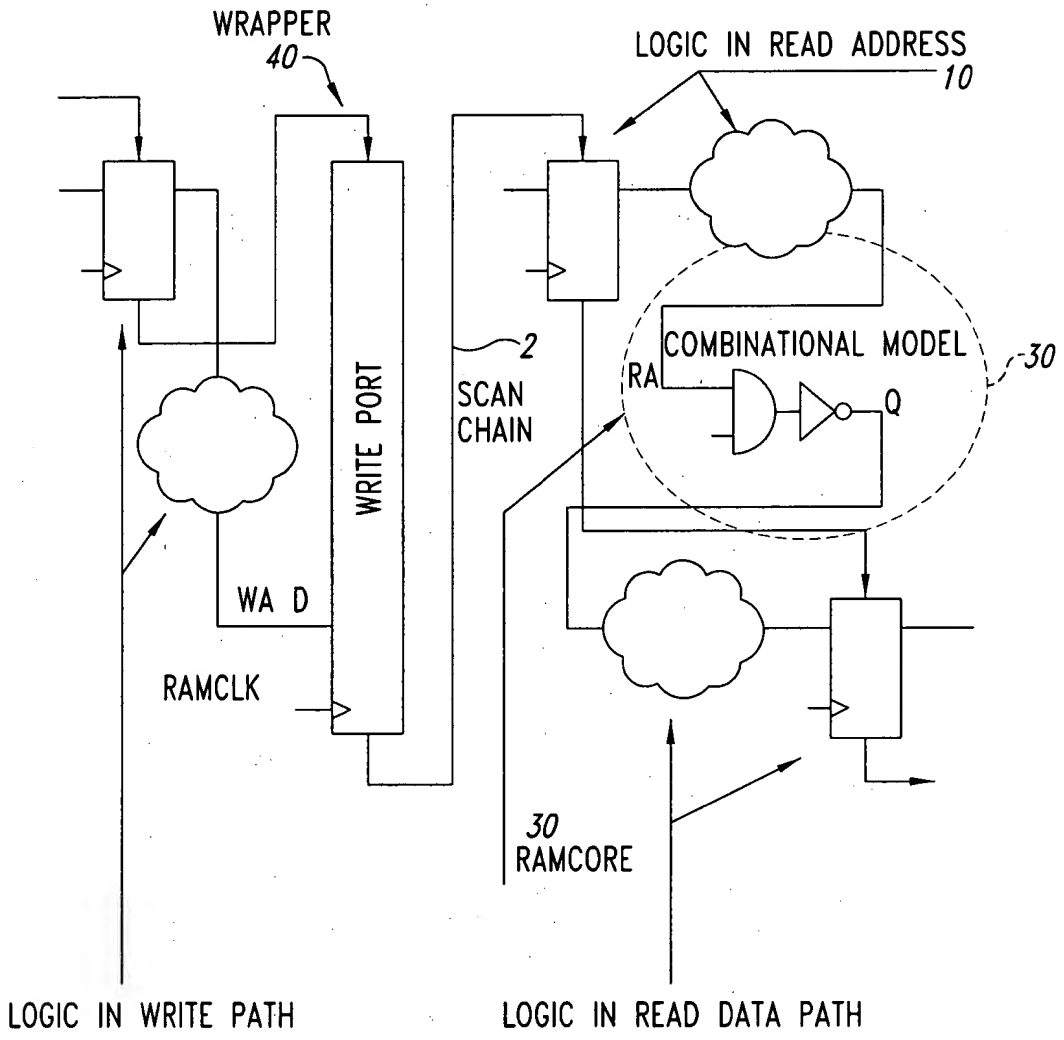
WRAPPER
40
LOGIC IN READ ADDRESS
10
WRITE PORT
2
SCAN
CHAIN
COMBINATIONAL MODEL
30
RA
Q
WA D
RAMCLK
30
RAMCORE
LOGIC IN WRITE PATH
LOGIC IN READ DATA PATH

*Fig. 12*